

a<sup>1</sup> "This is a counterpart of, and claims priority to, Japanese Patent Application No. 2000-010250, filed on Jan. 17, 2000, the contents of which are incorporated herein by reference."

[ Replace the paragraph beginning on page 9, line 21 with the following paragraph:

a<sup>2</sup> "A SiN sidewall layer, having a thickness from 100nm to 200nm, is formed on the semiconductor substrate using LP-CVD. An anisotropic etching technique, such as a RIE method, is employed to etch the SiN sidewall layer, so that SiN sidewalls 222 are formed as seen in fig. 6(c). (Step 55) Subsequent steps are the same as those in the first embodiment. (Steps 56-58)"

[ Replace the paragraph beginning on page 10, line 26 with the following paragraph:

a<sup>3</sup> "A SiN sidewall layer, having a thickness from 100nm to 200nm, is formed on the semiconductor substrate using LP-CVD. An anisotropic etching technique, such as a RIE method, is employed to etch the SiN sidewall layer, so that SiN sidewalls 322 are formed as seen in Fig. 9(b). (Step 84)"

[ Replace the paragraph beginning on page 14, line 1 with the following paragraph:

a<sup>4</sup> "A SiN sidewall layer, having a thickness from 100nm to 200nm, is formed on the

cont  
24

semiconductor substrate using LP-CVD. The formation of the SiN sidewall layer is performed at a temperature of over 850°C. In experiments, the inventors have shown that high temperature formation of the SiN sidewall reduces the hydrogen that diffuses into the semiconductor substrate. An anisotropic etching technique, such as a RIE method, is employed to etch the SiN sidewall layer, so that SiN sidewalls 522 are formed. (Fig. 15(b), Step S144)"

[ Replace the paragraph beginning on page 17, line 17 with the following paragraph:

25

"The gate electrode material 716 and the cap layer material 720 are formed on the gate oxide layer 724. A lithography method and an anisotropic etching technique, such as a RIE method, are employed to etch the gate electrode material 716 and the cap layer material 720. The gate electrode 716 and the cap layer are thereby formed. (Step S202)"

**In the Claims:**

Please cancel claims 16 and 18 without prejudice or disclaimer of the subject matter contained therein.

The following replacement claims are respectfully submitted:

- Ab
1. (Amended) A semiconductor device comprising:
- 22
- A